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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,943	10/04/2004	Max Ward Muterspaugh	PU010178	4974

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EXAMINER

RILEY, SHAWN

ART UNIT	PAPER NUMBER
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2838

DATE MAILED: 04/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

i. ✓

Office Action Summary	Application No.	Applicant(s)	
	10/509,943	MUTERSPAUGH, MAX WARD	
	Examiner	Art Unit	
	Shawn Riley	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) ____ is/are pending in the application.
4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-10, 12 and 13 is/are rejected.
- 7) ☒ Claim(s) 5 and 11 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>10/2004</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6-10 and 12-13 are rejected under 35 U.S.C. §102(b) as being fully anticipated by Marusik et al. (U.S. Patent 5,521,808). Marusik shows,¹ (in, e.g., the(ir) figure 3 and corresponding disclosure)

As to claim 1;

A switch mode power supply, comprising: source of a periodic input supply voltage (through 18); filter capacitor (50); power, switching semiconductor coupled to said

¹ Note claims will be addressed individually and the material in parentheses are the examiner's annotated comments. Further unless needed for clarity reasons, recited limitation(s), will be annotated only upon their first occurrence. Annotated claims begin with the phrase "As to claim". Claims that are not annotated are seen as having already had the invention(s) addressed previously in an annotated claim and may be repeated for convenience of the applicant/examiner. Bolded words/phrases indicate rejected material based 112 paragraph rejections. Underlined words/phrases indicate objected to material. For method claims, note that under MPEP 2112.02, the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claimed, then the method claimed will be considered to be anticipated by the prior art device. When the prior art device is the same as a device described in the specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986). Therefore the previous rejections based on the apparatus will not be repeated.

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source (192) and to said capacitor or generating periodic rectified supply current pulse in said semiconductor having a first transition in a first direction and a second transition at an opposite direction at a frequency related to that of said input supply voltage to develop an output supply voltage in said capacitor; a source of a first switch control signal (from 184) for conditioning said semiconductor to conduction prior to said first transition in a manner to provide for zero voltage switching in said semiconductor, during said first transition; and a comparator (58) responsive to a signal indicative of said output supply voltage (via 56) and to a signal at a reference level (via 208) for generating a second switch control signal for said semiconductor to produce said second transition of said current pulse that is modulated, in accordance with a difference between said output supply voltage and said reference level signal, said comparator having a positive feedback signal path that provides hysteresis (via, inter alia, 206 and 42) with respect to said output supply voltage.

As to claim 2;

The power supply according to Claim 1, wherein said first transition occurs, when a first difference between an instantaneous level of said input supply voltage and said output supply voltage is reached (via comparison of two voltages by 58, see, e.g., column 5 lines 39-50).

As to claim 3;

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The power supply according to Claim 1, wherein said hysteresis prevents said semiconductor from generating multiple current pulses in a given period of said input supply voltage in a manner to maintain the zero voltage switching (by definition, hysteresis prevents multiple signals by requiring a higher threshold to be reached before a switch occurs).

As to claim 4;

The power supply according to Claim 1, wherein said switching semiconductor comprises a series pass transistor (192 is a pass transistor).

As to claim 6;

The power supply according to Claim 4, wherein said first transition occurs, when a voltage, developed between a pair of main current conducting terminals of said transistor, changes polarity (based on input via 184/76).

As to claim 7;

The power supply according to Claim 4, wherein said input supply voltage is coupled to a control terminal of said transistor via a signal path that bypasses a main current conducting path in said transistor (via 51/52/56 and through 58/76/182) to generate said first switch control signal at said control terminal of said transistor.

As to claim 8;

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The power supply according to Claim 1, further comprising a rectifier (194/168/22/46/32/34) for rectifying a mains supply voltage to produce said input supply voltage having a sine-wave rectified waveform.

9. (original) A switch mode power supply, comprising: a source of a periodic input supply voltage; a filter capacitor; a power, switching transistor coupled to said source and to said capacitor for generating periodic rectified supply current pulse in said transistor having a first transition in a first direction and a second transition at an opposite direction at a frequency related to that of said input supply voltage to develop an output supply voltage in said capacitor; said input supply voltage being coupled to a control terminal of said transistor via a signal path that bypasses a main current conducting path in said transistor to generate a first switch control signal at said control terminal of said transistor for conditioning said transistor to conduction prior to said first transition in a manner to provide for zero voltage switching in said transistor, during said first transition; and a comparator responsive to a signal indicative of said output supply voltage and to a signal at a reference level for generating a second switch control signal for said semiconductor to produce said second transition of said current pulse that is modulated, in accordance with a difference between said output supply voltage and said reference level signal.

10. (original) The power supply according to Claim 9, wherein said transistor comprises a series pass transistor.

12. (original) The power supply according to Claim 9, wherein said signal path that bypasses said main current conducting path includes said comparator.

13.. (original) The power supply according to Claim 9, wherein said first transition occurs, when a voltage developed between a pair of main current conducting terminals of said transistor changes polarity.

Allowable Subject Matter

3. Claim 5 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and section 707.07(a) of the M.P.E.P.

5. The following is an examiner's statement of reasons for allowance: As to claim 5, no prior art uncovered anticipates or renders obvious applicant(s) claimed power supply including a series pass transistor is coupled in series with a rectifier for preventing said capacitor from discharging via said transistor, outside said rectified supply current pulse.

Further, as to claim 11, no prior art uncovered anticipates or renders obvious applicant(s) claimed power supply said series pass transistor is coupled in series with a rectifier for preventing said capacitor from discharging via said transistor, outside said rectified supply current pulse.

Conclusion

Any inquiry from other than the applicant/attorney of record concerning this communication or earlier communications from the Examiner should be directed to the Patent Electronic Business Center (EBC) at 1.866.217.9197. Any inquiry from a member of the press concerning this communication or earlier communications from the Examiner or the application should be directed to the Office of Public Affairs at 703.305.8341. Any inquiry from the applicant or an attorney of record concerning this communication or earlier communications from the Examiner should be directed to Examiner Riley whose telephone number is 571.272.2083. The Examiner can normally be reached Monday through Thursday from 7:30-6:00 p.m. Eastern Standard Time. The Examiner's Supervisor is Karl Easthom who can be reached at 571.272.1989. Any inquiry about a case's location, retrieval of a case, or receipt of an amendment into a case or information regarding sent correspondence to a case **should be**

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directed to 2800's Customer Service Center at 571.272.2815. Any papers to be sent by fax MUST BE sent to fax number **571-273-8300**. Any inquiry of a general nature of this application should be **directed to the Group receptionist** whose telephone number is 571.272.2800. Status information of cases may be found at <http://pair-direct.uspto.gov> wherein unpublished application information is found through private PAIR and published application information is found through public PAIR. Further help on using the PAIR system is available at 1.866.217.9197 (Electronic Business Center).

April 06



Shawn Riley
Primary Examiner